REMARKS

Examiner Ann T. Hoang is thanked for the thorough examination and search of the subject Patent Application.

All Claims are believed to be in condition for Allowance, and that is so requested.

Objections to the drawings because the numerical reference **280** has been used twice in **Fig. 2** have been corrected into reference number **820** as advised by the examiner.

Objections to the disclosure of the specification because of various errors as listed by the examiner have been appropriately corrected on page **1**, page **2**, page **9**, and page **25** as advised by the examiner.

Objections to claims because of various typing errors as listed by the examiner have been appropriately corrected as advised by the examiner.

Objections to claims **12**,**14**, **22**, **30** and **33** as listed by the examiner because the following phrases of the claims render the claims indefinite have been appropriately corrected.

> In claim 12, the phrase "e.g." used in lines 2 and 3 of the claim. In claim 14, the phrase "e.g.," used twice in line 3 and once in line 4 of the claim. In claim 22, the phrase "i.e." used in line 46 of the claim. In claim 30, the phrase "i.e." used in line 3 of the claim. In claim 33, the phrases "inter alia" used in line 10 of the claim and "i.e." used in lines 46 and 72 of the claim

Objection to claim **15** because of a typing error as listed by the examiner has been appropriately corrected as advised by the examiner.

Objections to claims **20-21** and **28-29** because there is insufficient antecedent basis for the limitation "said switching transistor function" in lines 2-3 of the claims have been appropriately corrected.

Objections to claims **22** and **30** because there is insufficient antecedent basis for the limitation "said driver switch firing" in lines 33, 37, and 53 of claim 22 and line 2 of claim 30 have been appropriately corrected.

Objection to claim **33** because the acronym "AVS" in line 19 of the claim should be defined has been appropriately corrected as advised by the examiner.

Reconsideration of the rejection of claims **1-6**, **12-16**, and **19-21**, rejected under 35 U.S.C. 102(b) as being anticipated by Ueda et al. (US 5,977,651) is requested, based on the following remarks:

Claims **1**, **15**, **17** and **20-21** have been amended.

New claims **34-36** have been added. No new matter has been added.

Claim **1** (currently amended) of the claimed invention teaches:

1. (currently amended): A circuit, realizing a driver device for secure and reliable firing of an igniter or squib, connecting said squib via a high-side electronic switch to a power source and via a low-side electronic switch to circuit ground, incorporating separate power supply parts for high voltage and low voltage domains and equipped with elaborate intrinsic diagnostics and online testing features for circuit protection and operation securing purposes, comprising:

a means for control of said firing, said diagnostics, and said online testing having a safing sensor signal input pin, four pins for voltage sense input signals, four pins for two pairs of current control output signals, and a ground pin;

a means for said high-side switching of said squib to said power source performing high-side switching transistor functions for said firing, for said diagnostics, and for said online testing;

a means for said low-side switching of said squib to said circuit ground performing low-side switching transistor functions for said firing, for said diagnostics, and for said online testing;

a means for said high voltage domain power supply;

a means for said low voltage domain power supply;

a means for secured supply of electrical energy to said means for said high-side switching derived from said high voltage domain;

a means for steered~~secured~~ supply of ~~electrical energy~~currents to said means for said low-side switching derived from said low voltage domain and controlled by one pair of said current control output signals;

a means for steered supply of currents to a means for driving said high-side switching means derived from said low voltage domain and controlled by the other pair of said current control output signals;

a means for driving said high-side switching means for said squib controlled by said means for control of firing, diagnostic and online testing and supplying drive current

to said high-side switching means either for the case of said diagnostic and online testing operations or for the case of said firing operation;and

a means for connecting said high-side switching means and said low-side switching means to said means for control of firing, diagnostic and online testing in order to execute said diagnostic measurement and online testing by said four voltage sense input signals whereby in said case of diagnostic and online testing operations a switchable and controllable current flow is initiated in conjunction with appropriate voltage measurements and resistance evaluations thereby strictly observing that no firing condition for said squib ~~are~~ is allowed to occur and whereby in ~~said~~ case of said firing operation a secure firing of said squib is always guaranteed.

In claim **1** the definitions of "means for control of said firing, said diagnostics, and said online testing", of "means for said high-side switching", of "means for said low-side switching", have been amended to better clarify the purpose of said means, especially by prescisely enumerating and naming input and output signals as shown and described in the disclosure. Furthermore two "means for steered supply of currents" have been singled out and renamed from former "means of secured supply of electrical energy", separated into its respective operations with regard to means for low-side and high-side switching. These new designations and definitions describe more precisely the function and the operation of the circuit, without introducing any new matter.

In regard of claim **1,** the claimed invention is different from the invention of Ueda et al. because Ueda et al. do not disclose

"a means for control of said firing, said diagnostics, and said online testing having a safing sensor signal input pin, four pins for voltage sense input signals, four pins for two pairs of current control output signals, and a ground pin"

as disclosed in claim **1** of the claimed invention.

Applicant respectfully disagrees that Ueda et al. show "a means for control of said firing, said diagnostics, and said online testing having a safing sensor signal input pin, four pins for voltage sense input signals, four pins for two pairs of current control output signals, and a ground pin" as the claimed invention does. Item 4 shown in FIG.1 from Ueda et al. and identified as COLLISION DETECTOR 4 fails to be equivalent to or to substitute said "a means for control of said firing, said diagnostics, and said online testing" from the invention of the applicant.

Ueda et al. shows in FIG.1 as item 4 a COLLISION DETECTOR 4 and teaches in (column 4, line 18-33):

The vehicle air-bag system of FIG.1 includes air bags, and drive circuits for the respective air bags. The drive circuits are connected across the backup capacitor 2. The drive circuits are connected to a COLLISION DETECTOR 4. The drive circuits serve to activate the respective air bags in response to an output signal of the collision detector 4. The COLLISION DETECTOR 4 has an acceleration sensor of a semiconductor type which serves to detect acceleration (deceleration) of a vehicle body. The COLLISION DETECTOR 4 also has a section for deciding whether or not the vehicle body collides with an object in response to the acceleration (the deceleration) detected by the acceleration sensor. When it is decided that the vehicle body collides with an object, the COLLISION DETECTOR 4 outputs a low-level signal as a COLLISION DETECTION signal. Otherwise, the COLLISION DETECTOR 4 outputs a high-level signal.

Furthermore in (column 5, lines 9-18) is teached:

An NPN transistor 14 serves to drive the power transistor 13. The transistor 14 is referred to as the drive transistor 14. The base of the drive transistor 14 is connected to an output terminal of the COLLISION DETECTOR 4. The emitter of the drive transistor 14 is grounded. The collector of the transistor 14 is connected to the gate of the power transistor 13. When the COLLISION DETECTOR 4 outputs a low-level signal (a COLLISION DETECTION signal) to the drive transistor 14, the drive transistor 14 falls into an off state so that the power transistor 13 can change to its on state.

Further described in (column 6, lines 22-27):

In the absence of a collision of the vehicle body against an object, the COLLISION DETECTOR 4 outputs a high-level signal to the base of the transistor 14 so that the transistor 14 is in its on state. Accordingly, in this case, a low-level signal is applied to the gate of the power transistor 13, and the power transistor 13 is in its off state.

And further explained in (column 6 , lines 61-67):

In the event of a collision of the vehicle body against an object, the COLLISION DETECTOR 4 outputs a low-level signal (a collision detection signal) to the base of the transistor 14 so that the transistor 14 falls into its off state. Accordingly, in this case, a high-level signal is applied to the gate of the power transistor 13, and the power transistor 13 falls into its on state.

Finally in (column 7 , lines 1-3) is teached:

In the event of a collision, the safing sensor switch 12 falls into an on state (a closed state) before the COLLISION DETECTOR 4 outputs a COLLISION DETECTION signal.

It is obvious that in regard of the teachings of Ueda et al. the COLLISION DETECTOR 4 does not disclose serving as "means for control of said firing, said diagnostics, and said online testing having a safing sensor signal input pin, four pins for voltage sense input signals, four pins for two pairs of current control output signals, and a ground pin" as the claimed invention does. The COLLISION DETECTOR 4 according to the teachings of Ueda et al. solely performs the function of delivering a COLLISION DETECTION signal as output, i.e. "outputs a low-level signal as a COLLISION DETECTION signal".

As a consequence, it can be understood from the above that said COLLISION DETECTOR 4 from Ueda et al. is not delivering and not receiving any other control or sense signals other than said COLLISION DETECTION signal, such as those signals received and delivered of the claimed invention via said "four pins for voltage sense input

signals, four pins for two pairs of current control output signals" of said "means for control of said firing, said diagnostics, and said online testing" as claim **1** of the claimed invention requires.

Furthermore, Ueda et al. do not disclose using more than one controlled current source as the claimed invention does, as comprised in those two "means for steered supply of currents" teached from claim **1** of the invention of the applicant

"a means for steered supply of currents to said means for said low-side switching derived from said low voltage domain and controlled by one pair of said current control output signals;
a means for steered supply of currents to a means for driving said high-side switching means derived from said low voltage domain and controlled by the other pair of said current control output signals;"

and more precisely elaborated in claims **17**, **34-36** of the claimed invention.

Claim **17** (currently amended) of the claimed invention teaches:

17. (currently amended): The circuit according to claim **1** wherein said means for steered~~secured~~ supply of ~~electrical energy~~currents to said low-side switching means derived from said low voltage domain consists of ~~two~~ one pair of controlled current sources fed by voltages out of said low voltage domain for controlled current switching between different currents for current limiting and diagnostic testing purposes respectively.

Claims **34-36** (new) of the claimed invention teach in more detail:

34. (new): The circuit according to claim **1** wherein said means for steered supply of currents to a means for driving said high-side switching means derived from said low voltage domain consists of one pair of controlled current sources fed by voltages out of

said low voltage domain for controlled current switching between different currents for current limiting and diagnostic testing purposes respectively.

35. (new): The circuit according to claim **34** wherein one current source of said pair of controlled current sources is used in case of said diagnostic and online testing operations and the other current source is used in case of said firing operation and each current source is being controlled by a separate case related current control input and whereby as current output from said pair of controlled current sources one common output is formed.

36. (new): The circuit according to claim **17** wherein one current source of said pair controlled current sources is used in case of said diagnostic and online testing operations and the other current source is used in case of said firing operation and each current source is being controlled by a separate case related current control input and whereby as current output from said pair of controlled current sources one common output is formed.

As can be understood from claim **1** and claims **17**, and **34-36** above at least four separate controlled current sources are used within the invention of the applicant.

Ueda et al. disclose only using multiple constant-current sources, which are not controlled however. A controlled current source is essentially a three-pole device, a constant-current source is essentially a two-pole device, which Ueda et al. confirm by designating only a "first end of the constant-current source" as a first pole and a " second end of the constant-current source" as a second pole, no third pole items as part of three-pole devices are disclosed.

Ueda et al. teach in (column 9, lines 25-55):

A first end of the constant-current source 21k is connected to a constant-voltage line subjected to the stabilized DC voltage Vcc. A second end of the constant-current source 21k is connected to the emitters of the transistors 21d and 21g. The base of the transistor 21d is connected to the inverting input terminal 21a. The base of the transistor 21g is

connected to the non-inverting input terminal 21b. The collector of the transistor 21d is connected to the collector of the transistor 21e. The bases of the transistors 21e and 21f are connected to each other. The collector of the transistor 21d is connected to the bases of the transistors 21e and 21f. The emitters of the transistors 21e and 21f are grounded. The collector of the transistor 21g is connected to the collector of the transistor 21f.

A first end of the constant-current source 21l is connected to the constant-voltage line subjected to the stabilized DC voltage Vcc. A second end of the constant-current source 21l is connected to the emitter of the transistor 21h and the base of the transistor 21i. The base of the transistor 21h is connected to the junction between the collectors of the transistors 21g and 21f. The collector of the transistor 21h is grounded.

A first end of the constant-current source 21m is connected to the constant-voltage line subjected to the stabilized DC voltage Vcc. A second end of the constant-current source 21m is connected to the collector of the transistor 21i. The emitter of the transistor 21i is connected to the base of the transistor 21j. The emitter of the transistor 21i is grounded via the resistor 21p. The collector of the transistor 21j is connected to the output terminal 21c. The emitter of the transistor 21j is grounded.

Ueda et al. teach furthermore in (column 10, lines 54-65):

A first end of the constant-current source 24n is connected to a constant-voltage line subjected to the stabilized DC voltage Vcc. A second end of the constant-current source 24n is connected to the emitters in the transistor set 24l. The collectors in the transistor set 24l are connected to the emitters of the transistors 24f and 24i. The base of the transistor 24f is connected to the base of the transistor 24e and the collector of the transistor 24e. The emitter of the transistor 24e is connected to the emitter of the transistor 24d. The base of the transistor 24d is connected via the resistor 24p to the non-inverting input terminal 24b. The collector of the transistor 24d is grounded.

Ueda et al. teach finally in (column 11, lines 5-14):

A first end of the constant-current source 24o is connected to the constant-voltage line subjected to the stabilized DC voltage Vcc. A second end of the constant-current source 24o is connected to the emitters in the transistor set 24m. A first collector in the transistor set 24m is connected to the base of the transistor 24f, the collector of the transistor 24e, and the base of the transistor 24e. A second collector in the transistor set 24m is connected to the base of the transistor 24i, the collector of the transistor 24h, and the base of the transistor 24h.

As can be understood from the above cited sections from Ueda et.al. there are only "first and second ends" of said constant-current sources disclosed in Ueda et.al., i.e.

no three-pole devices and therefore none of the cited constant-current sources is controllable.

Only within one paragraph (column 12, line 26-32) in Ueda et al. a single "constant-current source 20" is disclosed which can be "externally adjusted".

The constant-current source 20 may be designed so that the value of the regulated current provided thereby can be adjusted in accordance with an externally-fed instruction. Alternatively, the constant-current source 20 may adjust the value of the regulated current in response to a command value fed from a suitable memory such as a nonvolatile memory.

In regard of claim **1,** and in view of claims **17**, **34-36** the claimed invention is different from the invention of Ueda et al. because Ueda et al. do not disclose a circuit comprising more than one controlled current-source, whereas the claimed invention comprises at least four controlled current-sources as can be understood from the above.

Applicant believes claim **1** of the claimed invention to be patentable because of the differences between the claimed invention and the disclosure of Ueda et al. shown above.

Claims **2 - 6** are dependent claims upon base claim **1** which is believed to be patentable according the arguments above.

Claims **12 - 16** are dependent claims upon base claim **1** which is believed to be patentable according the arguments above.

Claims **19 - 21** are dependent claims upon base claim **1** which is believed to be patentable according the arguments above.

Reconsideration of the rejection of claim **18** as being unpatentable over Ueda et al. (US 5,977,651) in view of Abe (US 2002/0125950) under 35 U.S.C. 103(a) is requested, based on following remarks:

Claim **18** is a dependent claim upon base claim **1** which is believed to be patentable according the arguments above.

New Claims **34** to **38** have been added. No new matter has been added.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

We therefore politely request examiner Ann T. Hoang to reconsider his rejection in view of these arguments.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now allowable that the Examiner call the undersigned at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761

AMENDMENTS TO THE DRAWINGS:

The attached sheet of drawings includes changes to **FIG. 2**. This sheet, which shows **FIG. 2**, replaces the original sheet showing **FIG. 2**. In the original drawing of **FIG. 2** showing a circuit diagram, the reference item number **820** was erroneously shown as **280**. This has been corrected.

Attachment: Replacement sheet